



2002 Analyst Meeting

November 7, 2002

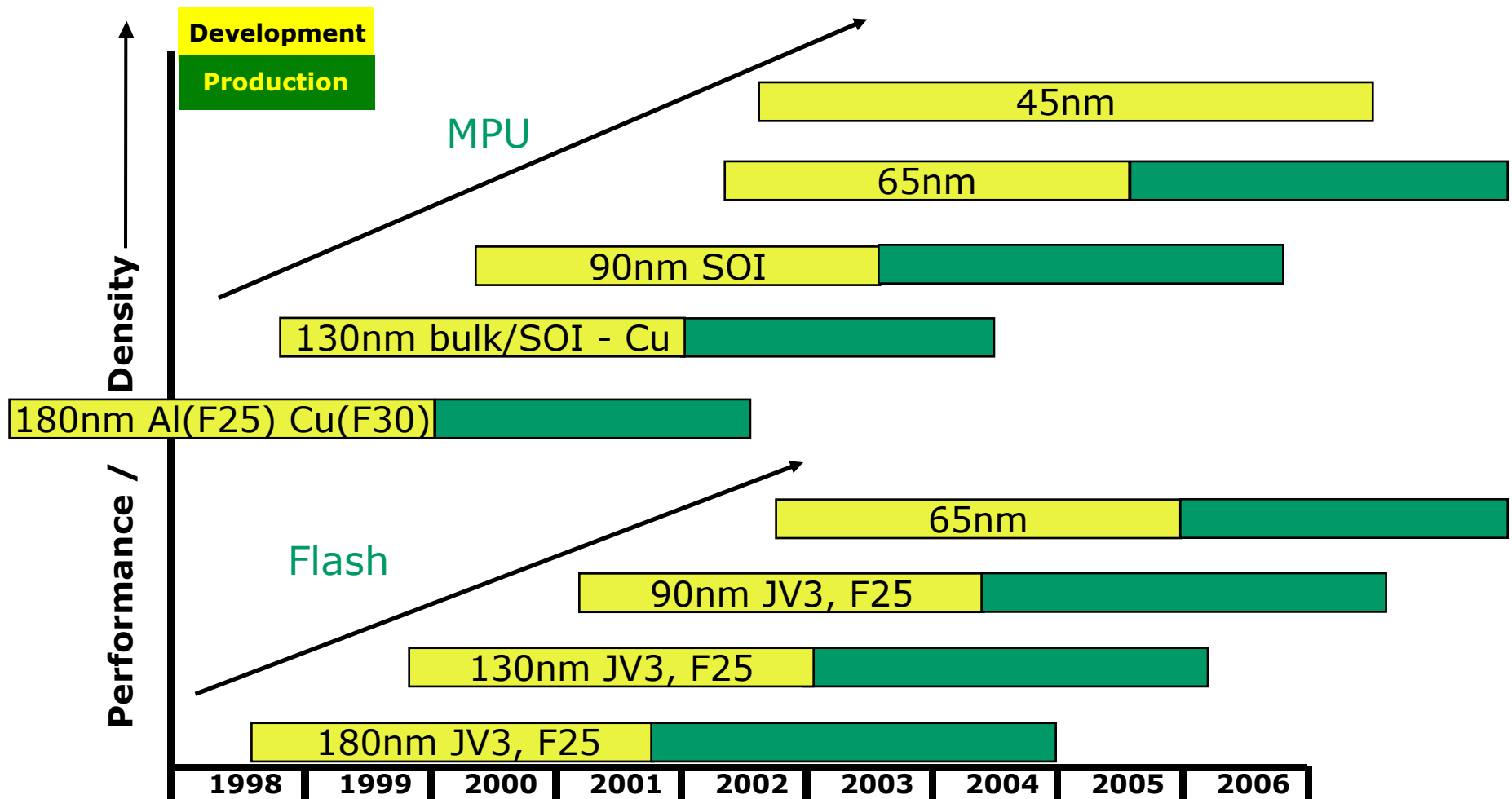


Bill Siegle
SVP, Technology Operations and
Chief Scientist

November 7, 2002

- 130nm
 - Complete Fab30 transition to 130nm by 3Q'02 – Done
 - Prepare for 130nm Flash introduction in JV3, F25
- 90nm
 - Qualify Hammer on 90nm (HiP8) in 2H03 (Fab30)
 - Fully convert Fab30 to 90nm by 2H'04
 - Initiate 90nm flash production in 2H04
- 65nm
 - Initial development on 200mm now
 - Shift logic development to 300mm during 2003
 - Qualify first production by 2H05, both logic and flash
- 45nm
 - Research projects underway

Technology Roadmap



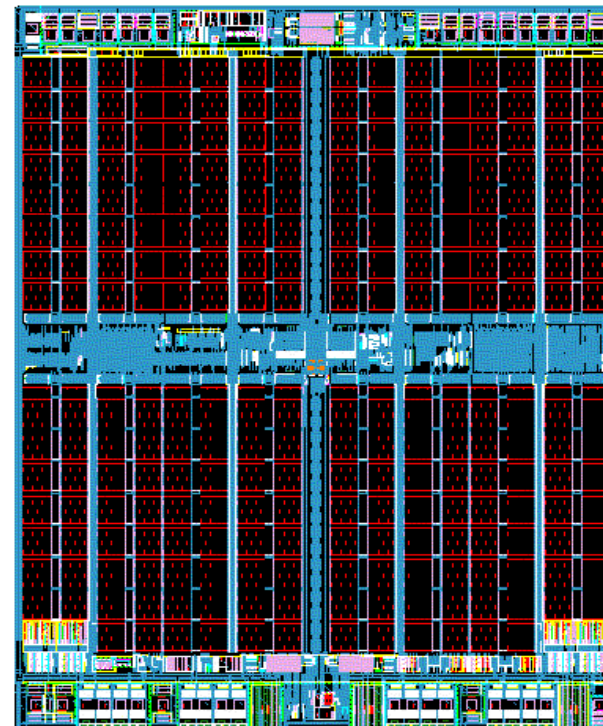
Memory Technology

130nm Flash



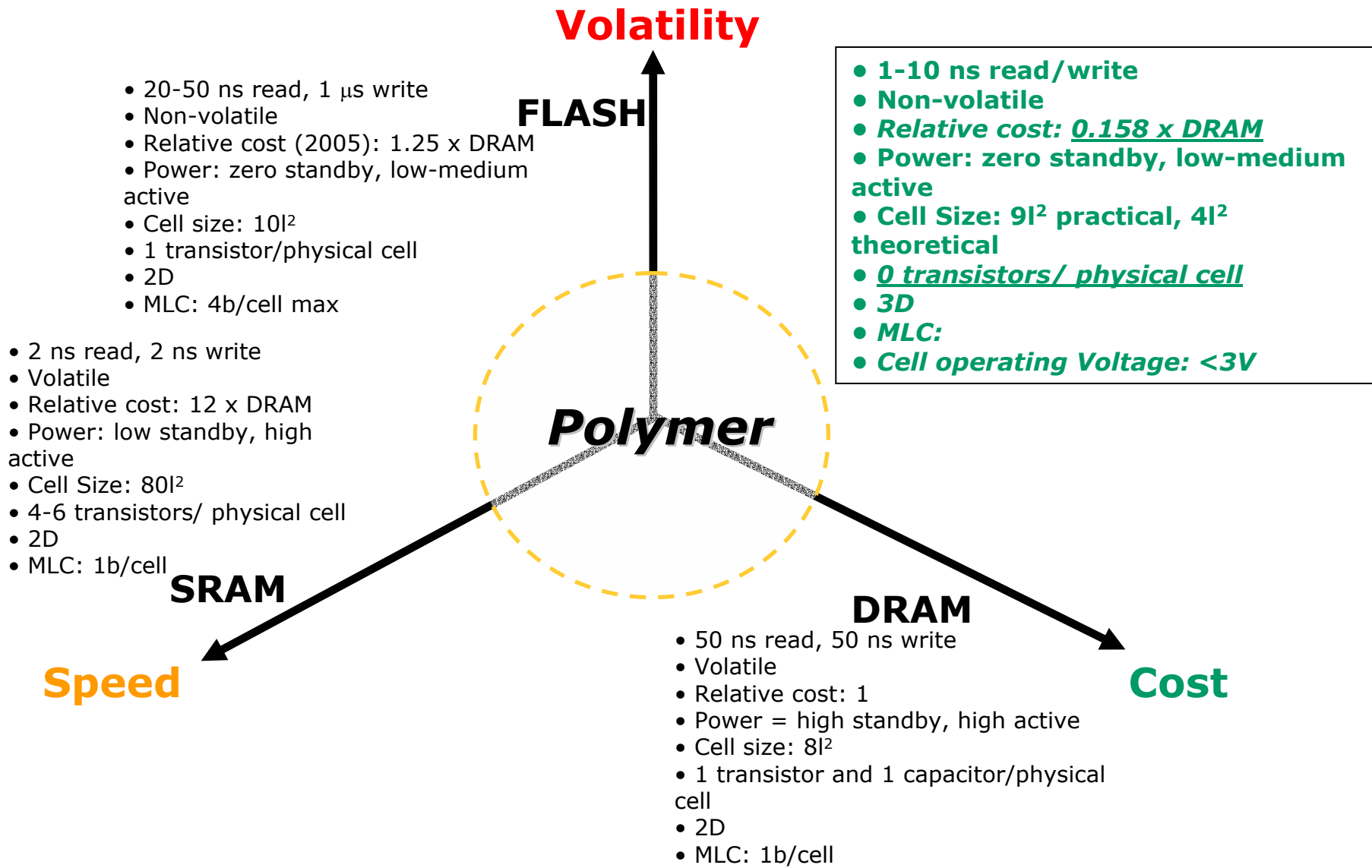
- CS69 130nm Flash Memory
 - Technology Development in Sunnyvale
 - Parallel release to manufacturing in F25 (Austin) and JV3 (Aizu)
 - Production ship Q1
- 130nm Mirror Bit
 - Production ship 2H'03
- 90nm in development
 - Production in 2004

1.8v AMD 64Mb Burst

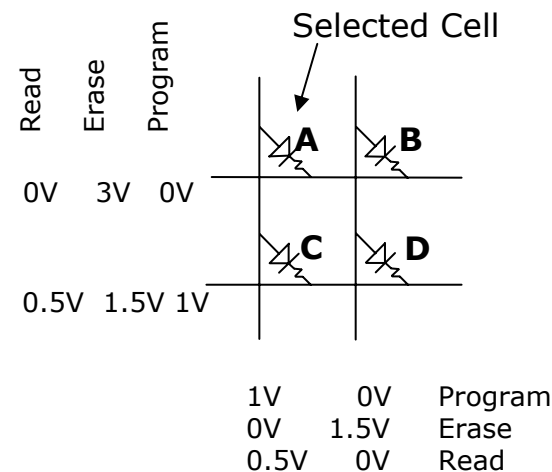
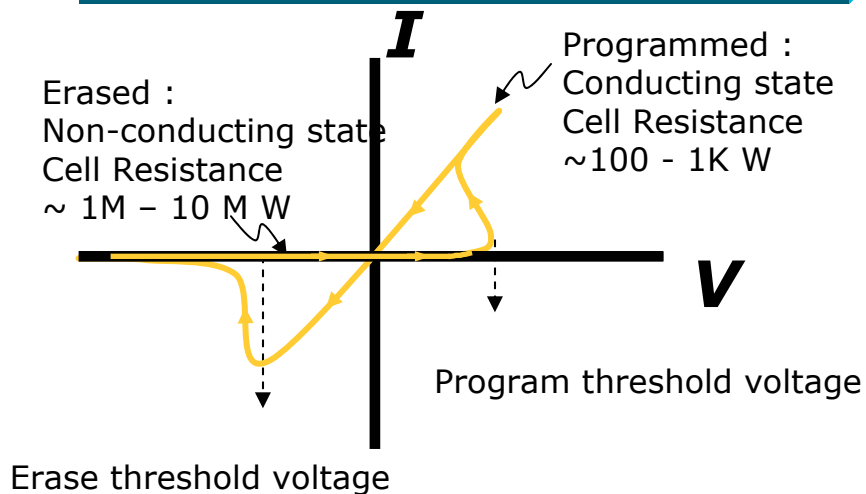
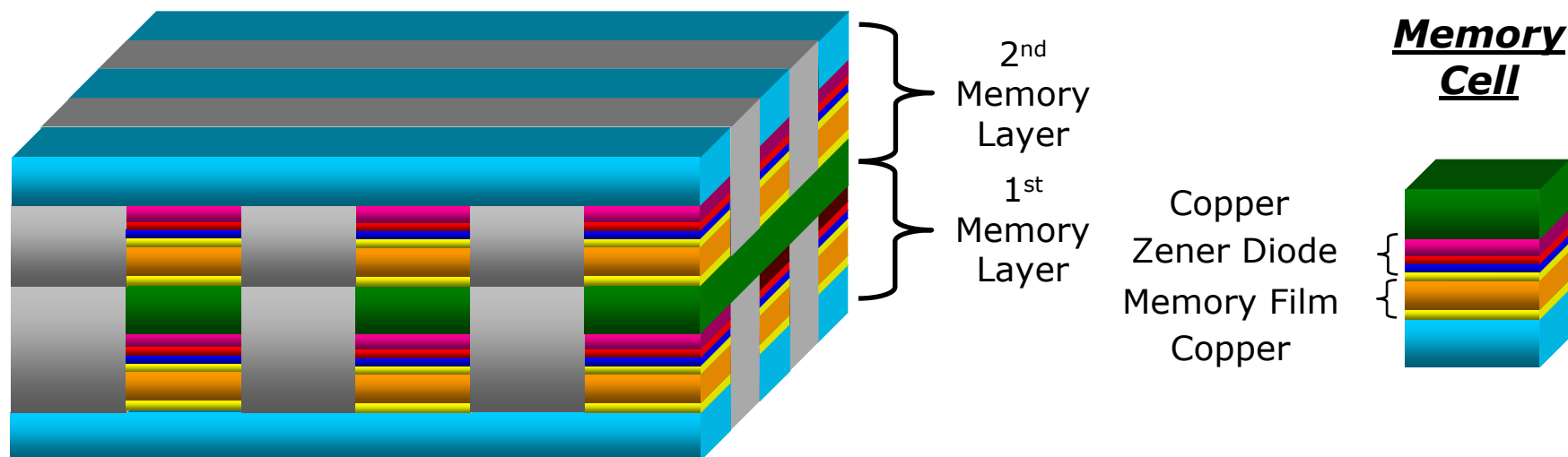


CS69

The Ultimate Memory Solution?



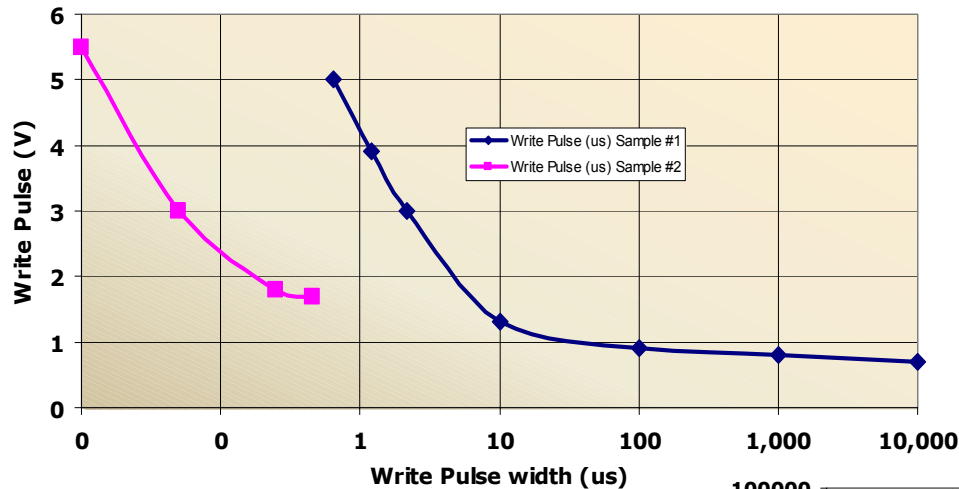
Cell and Array Cross-section



Write Speed vs. Voltage

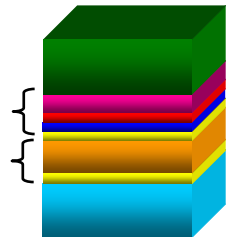


Write Pulse (us) vs. Voltage

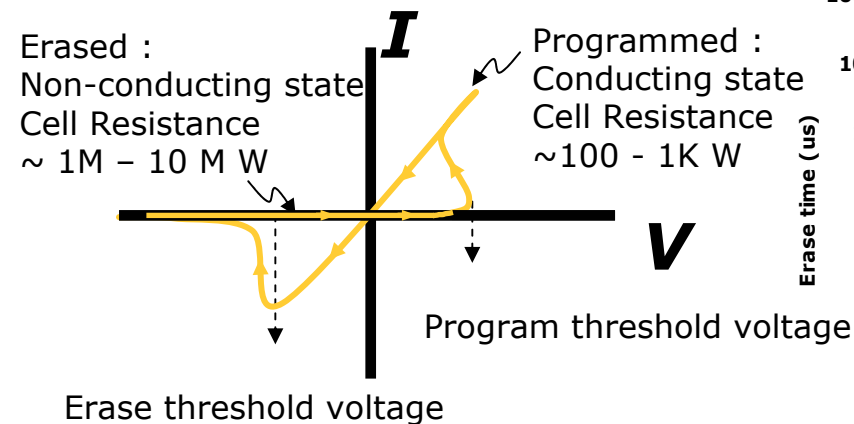
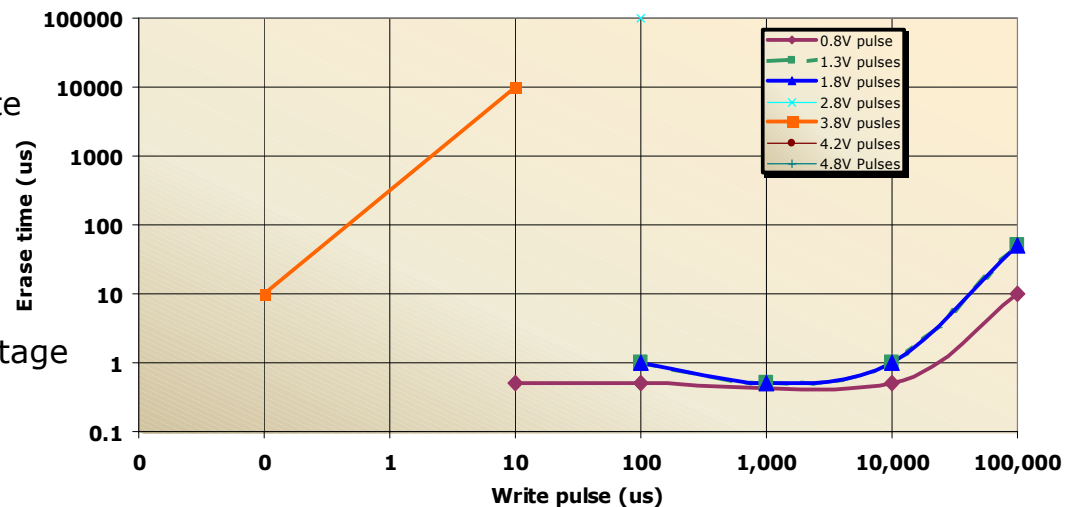


Memory Cell

Copper
Zener Diode
Memory Film
Copper

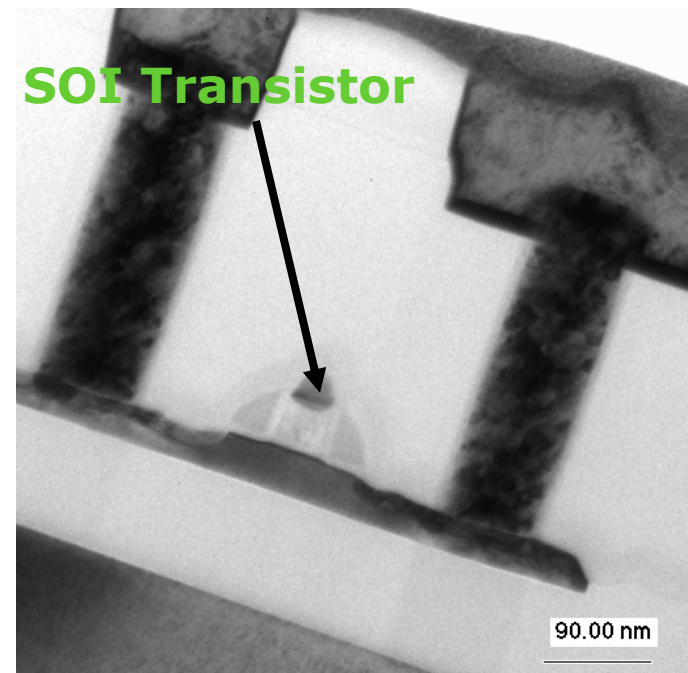


Erase time vs. Write pulse

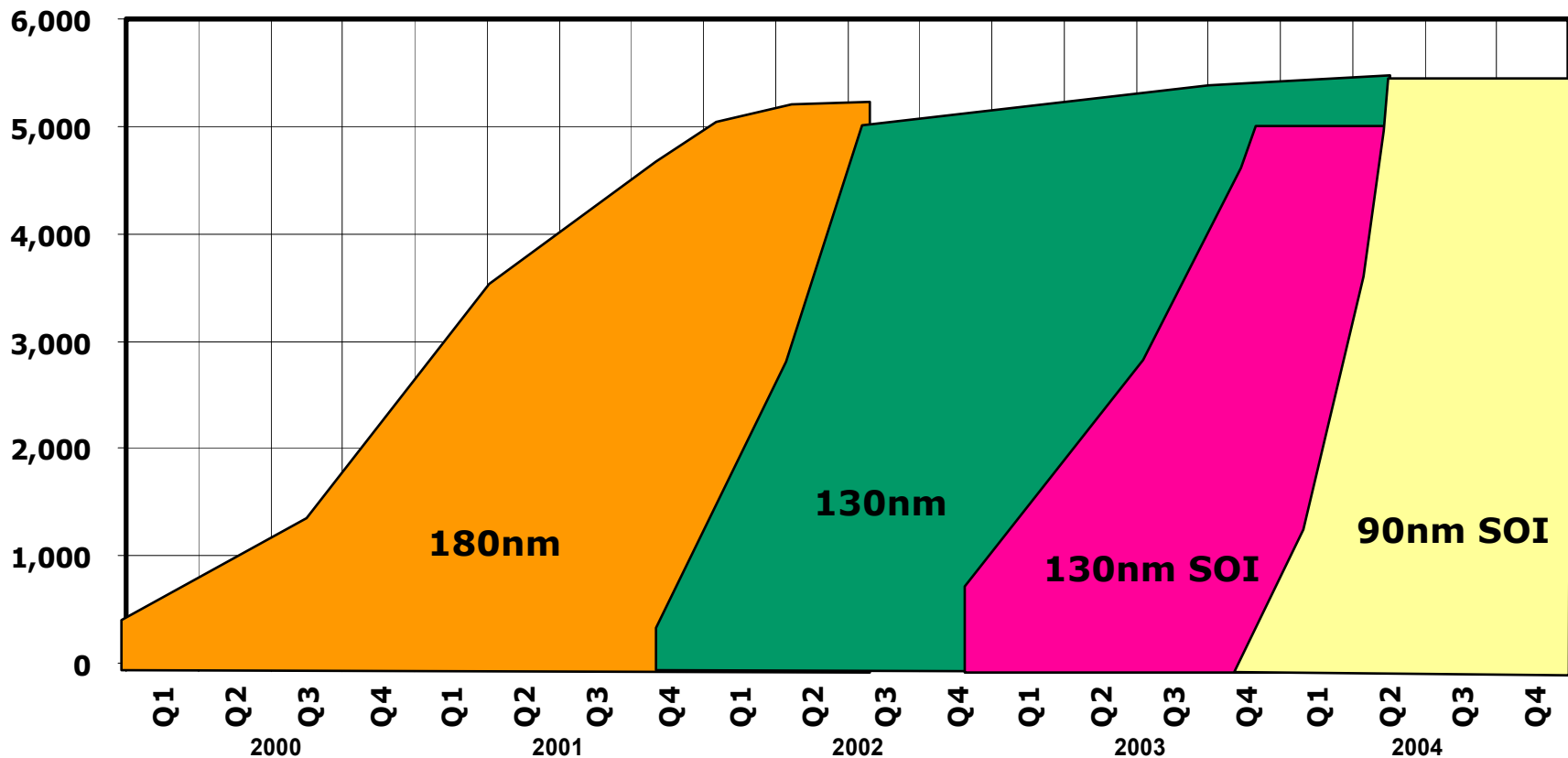


Logic Technology

- F30, Dresden
 - 100% converted to 130nm for Athlon production
 - Running >5000 w/wk
 - Preparing for SOI based Hammer family introduction

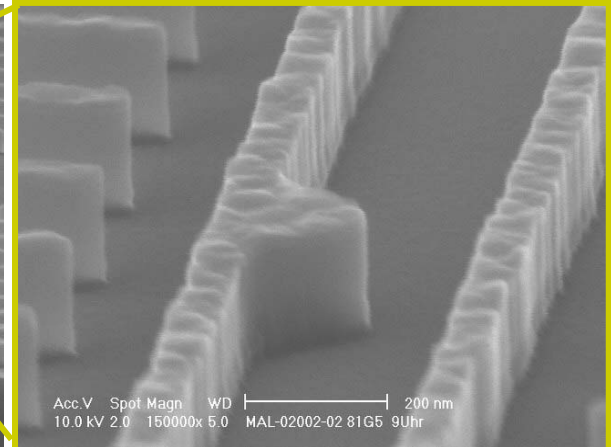
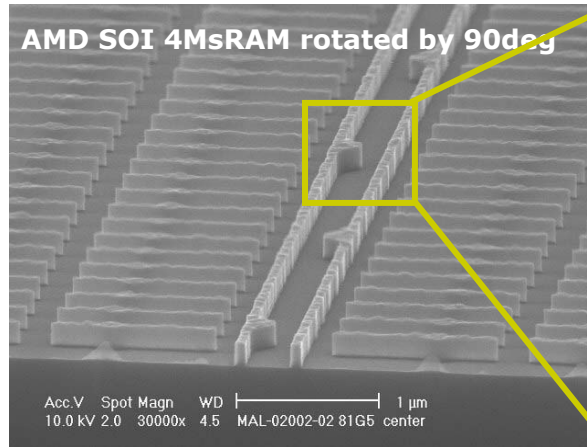
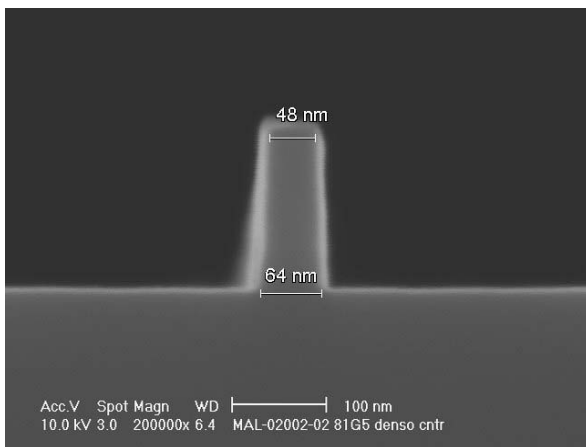
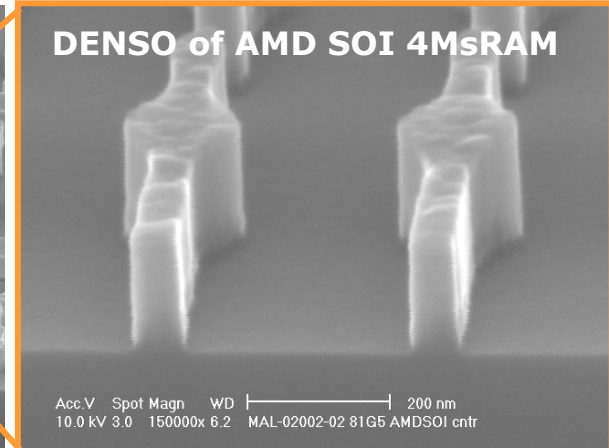
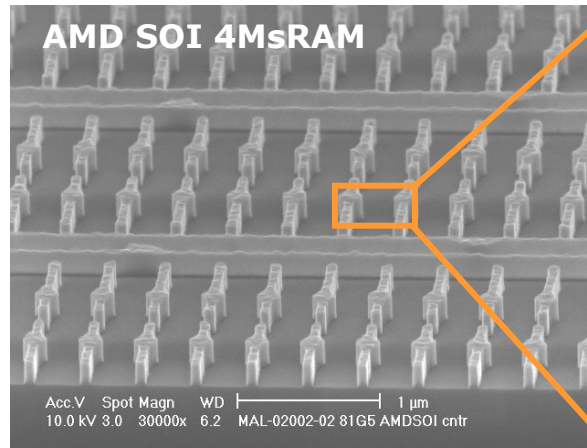
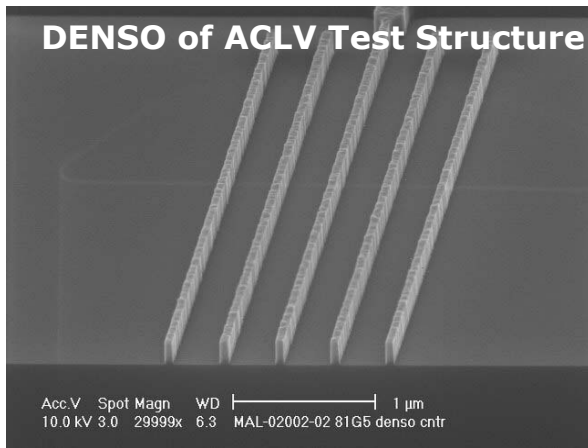


Fab 30 Wafer Starts

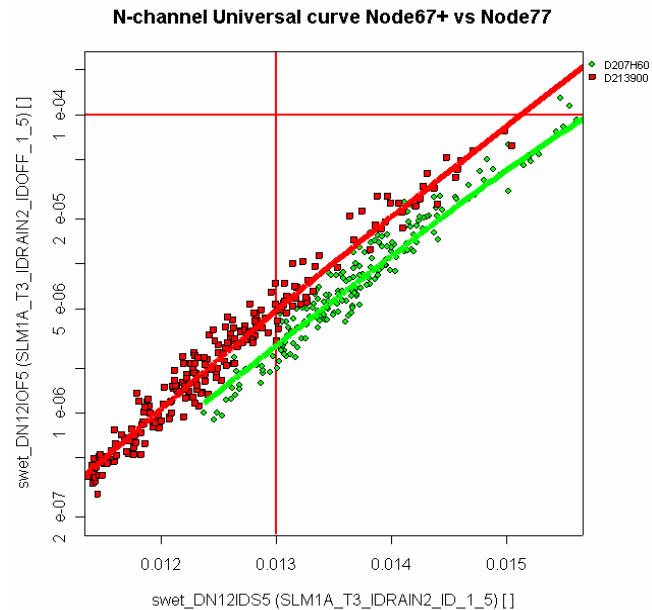
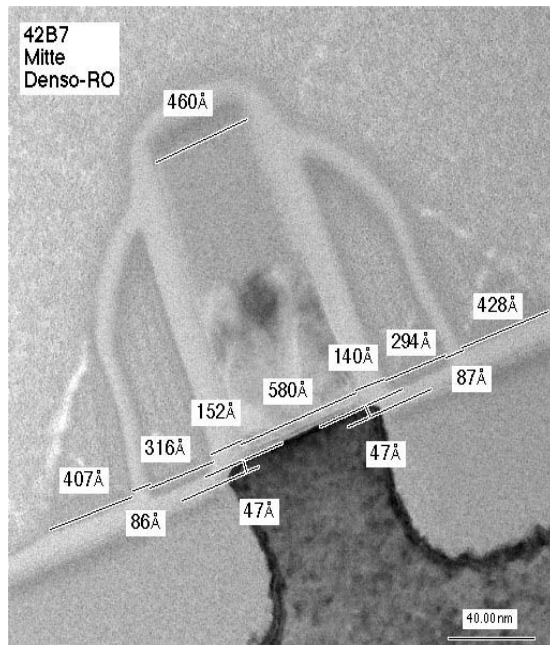


- Early development carried out in AMD/Motorola Alliance in Austin
- Activity transferred to Dresden, Fab30 in 2Q02
- Technology development vehicle (4Mb SRAM) running today in Fab
- Initial SledgeHammer vehicle now in tape-out

90nm SRAM Gate patterning: SEM



Improved speed with triple spacer



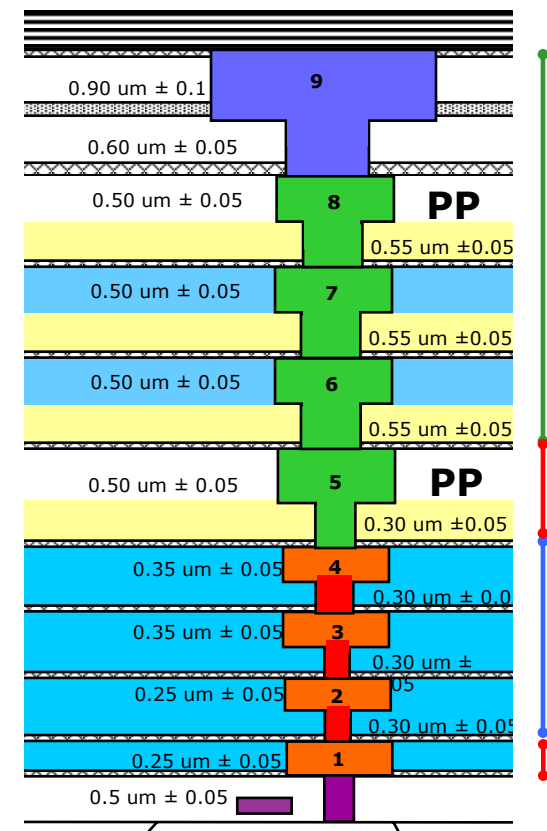
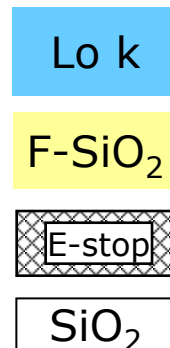
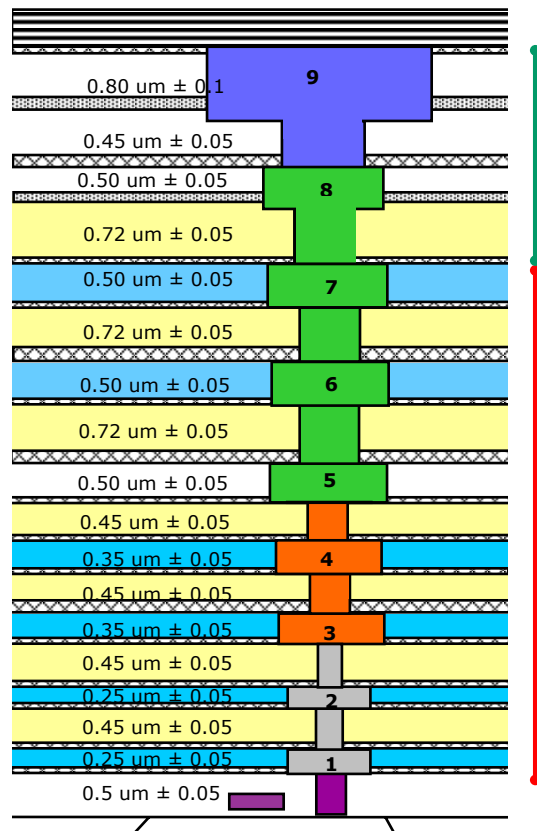
- “Triple Spacer” concept provides improved transistor performance,

BEOL Evolution 130nm through 90nm



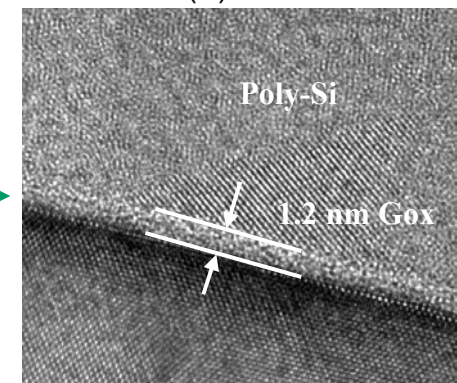
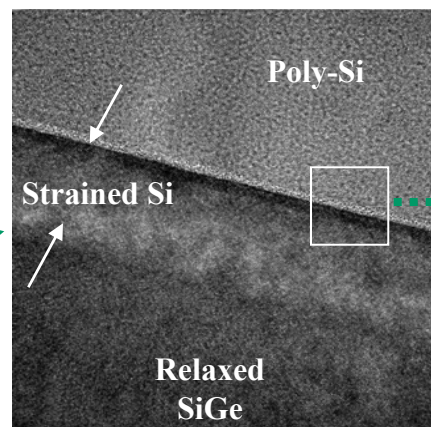
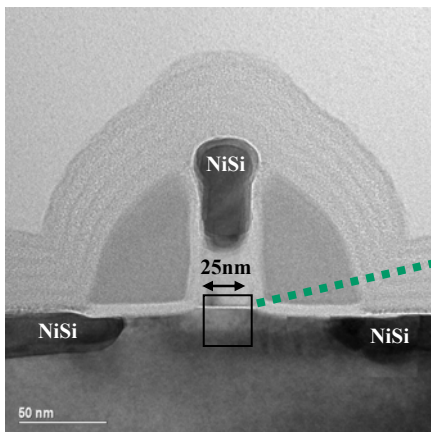
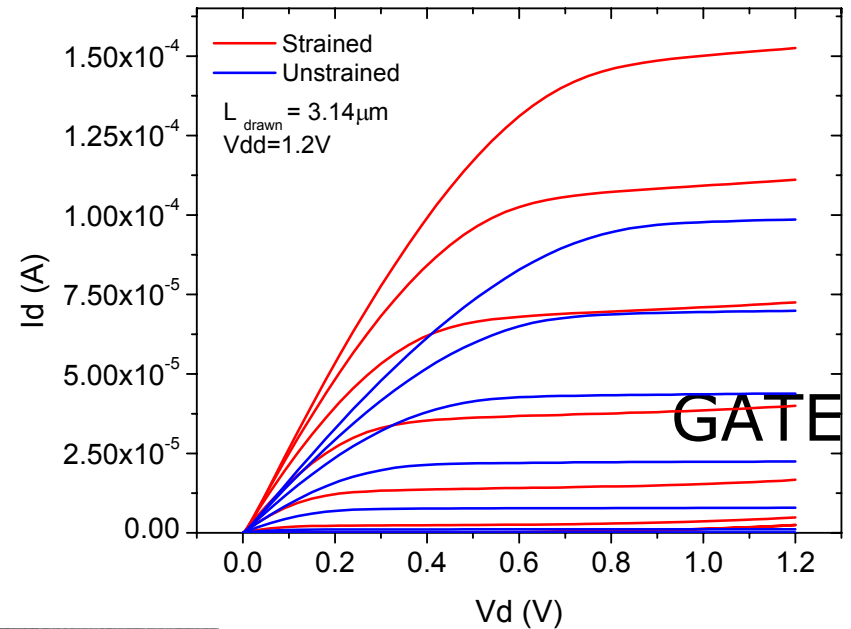
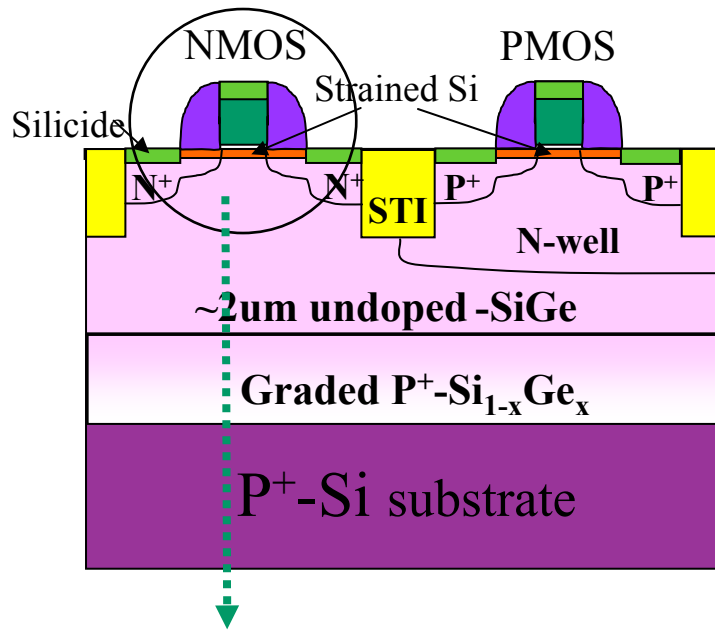
- 130nm starting BEOL
- Currently running in F30

- Improved interconnect stack for 90nm
- Technology ready by 12/2002
- Production in 2H/2003



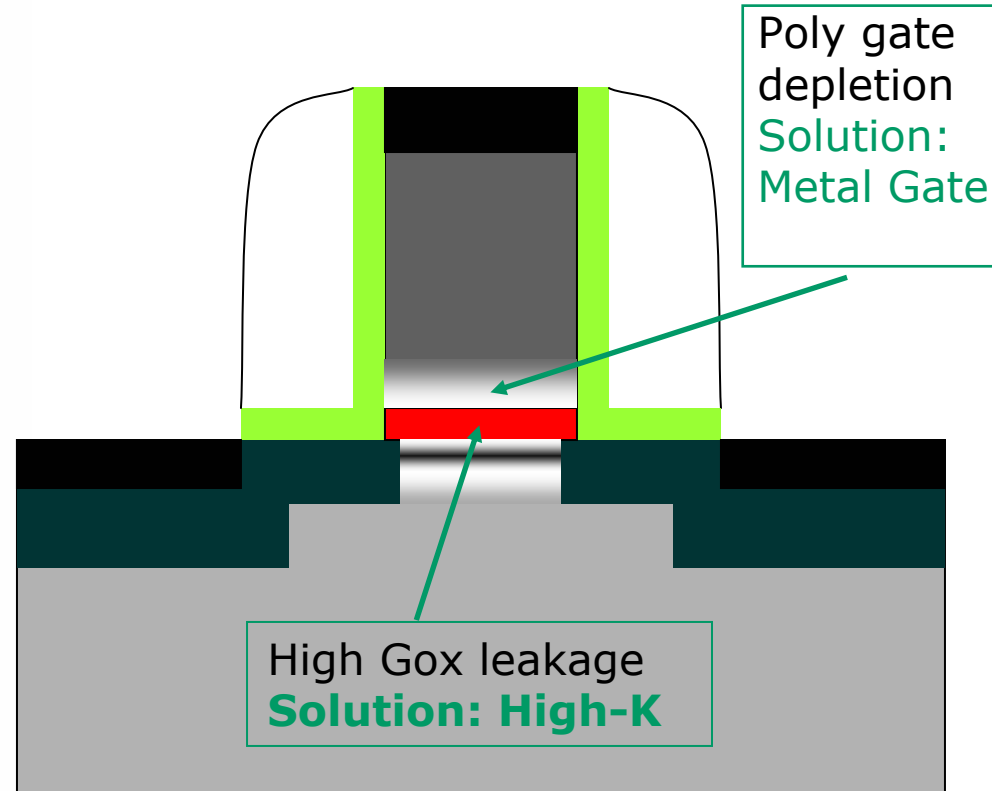
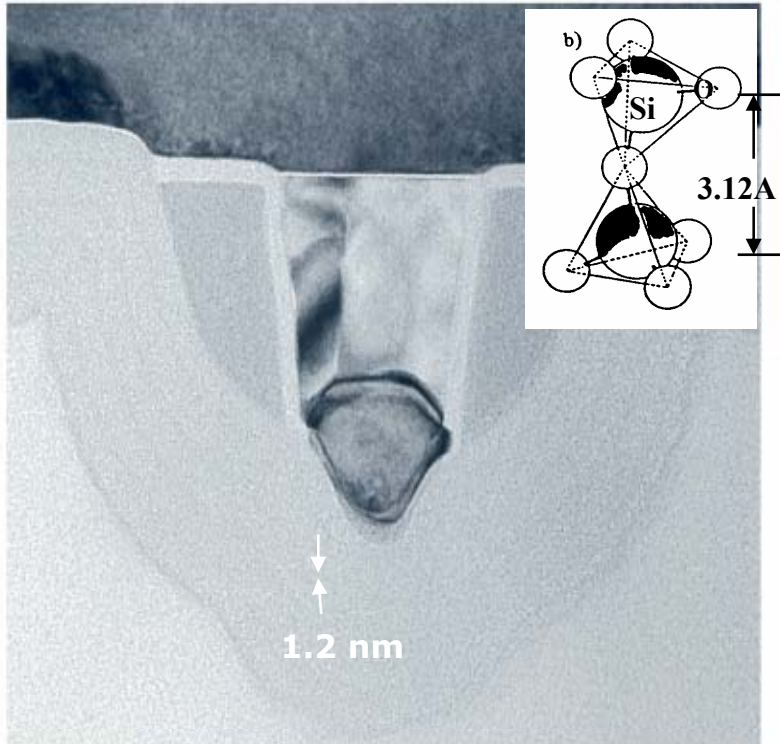
- Technology options currently under study
- Will converge over the next year to a “baseline” technology choice and process flow
- Exercise with test vehicle in '03, follow with product-like vehicles in '04
- Production qualification 2H'05

Strained-Si Transistors



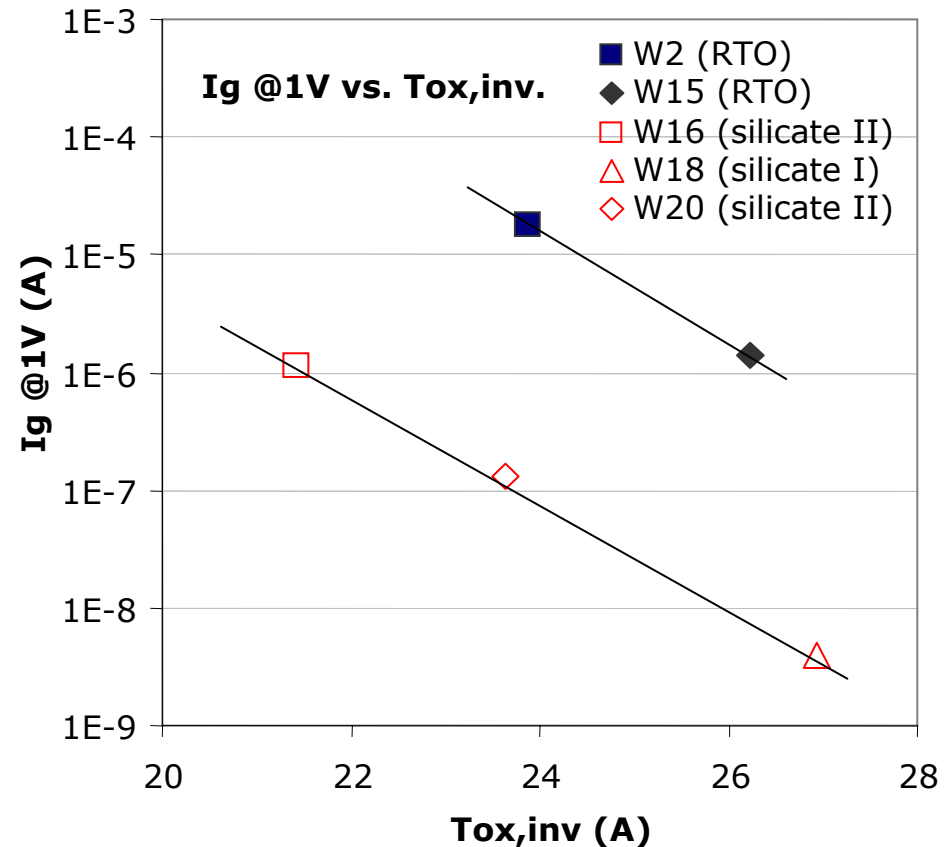
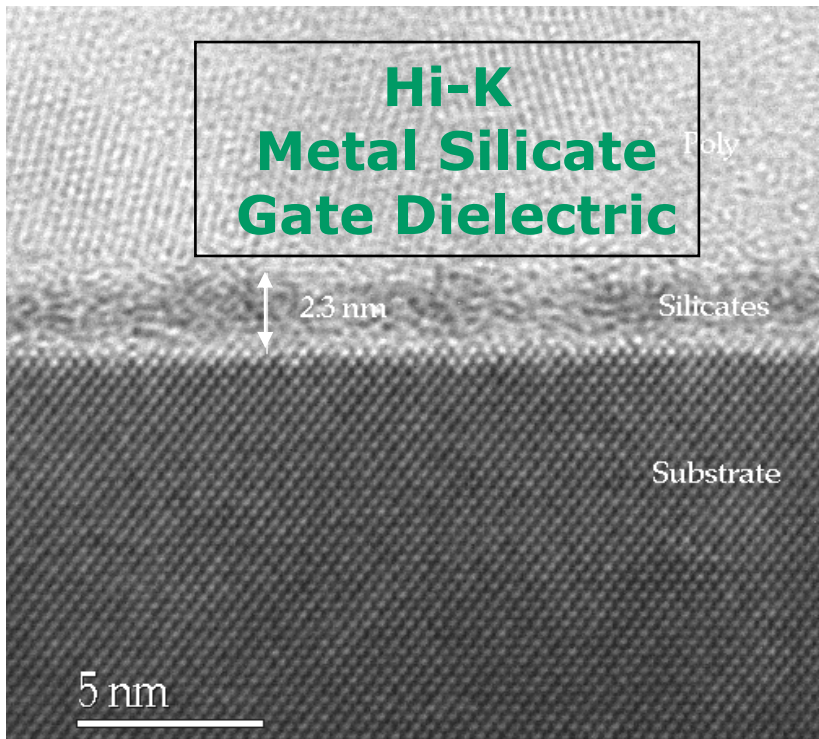
Strained substrate: 20% Ge; 175Å strained Si

Is there any oxide left?

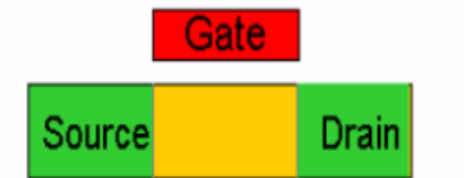


longer behaves as a good insulator

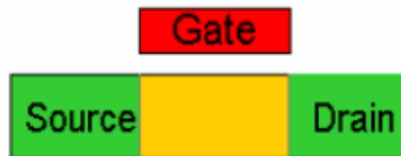
- Need to reduce gate leakage and increase gate capacitance
- **High dielectric constant** -> Same capacitance, but lower gate leakage



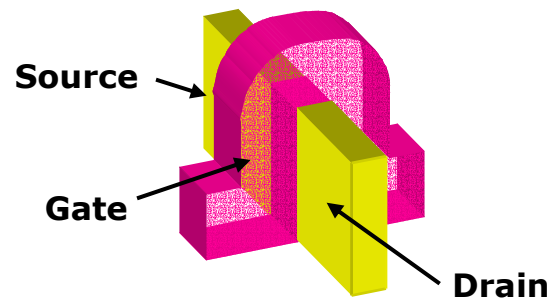
- For the same inversion Tox , Metal-silicate show 2 order less leakage than SiO_2 control



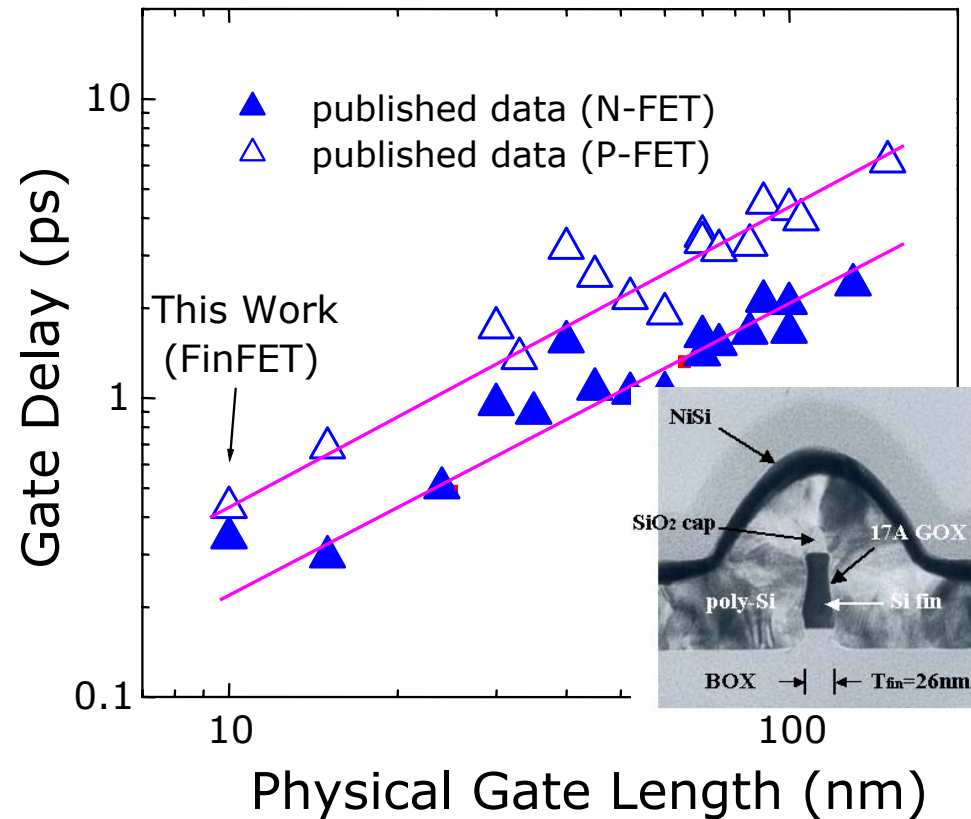
Conventional Single Gate



Dual Gate



Fin-FET

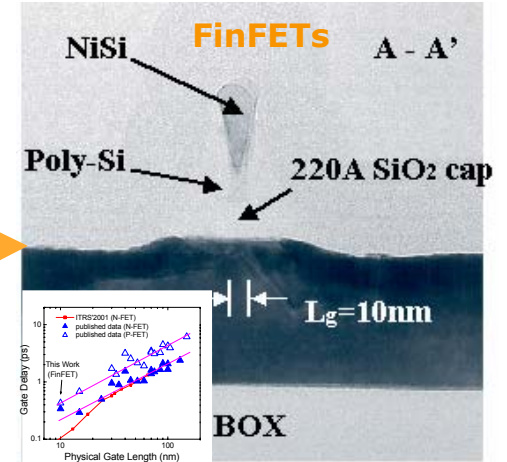
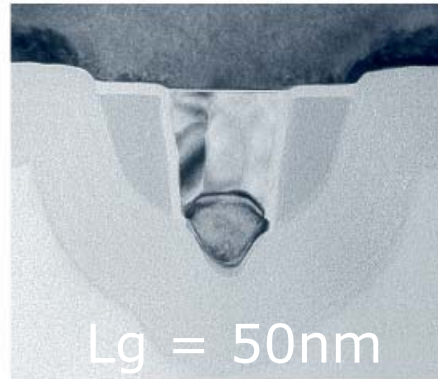
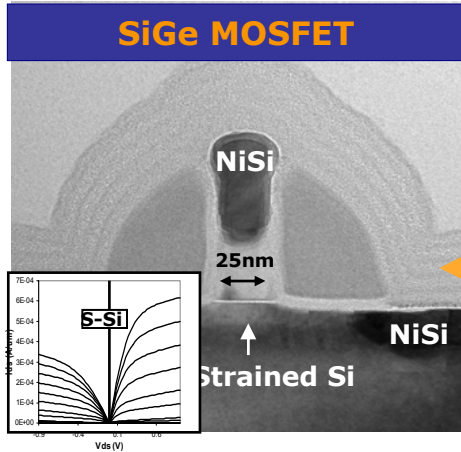


•Good short-channel behavior

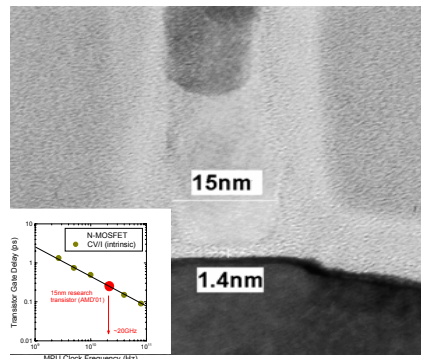
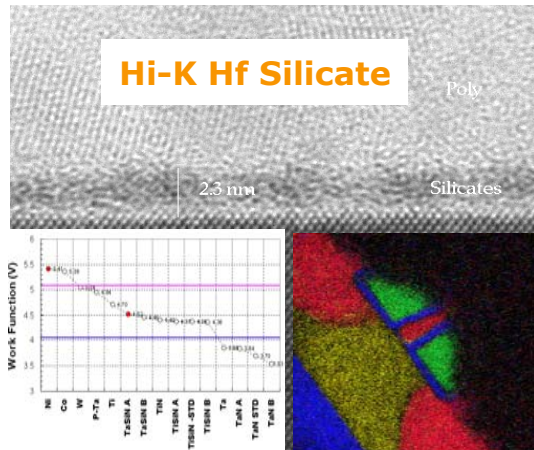
Path to < 15nm Transistors



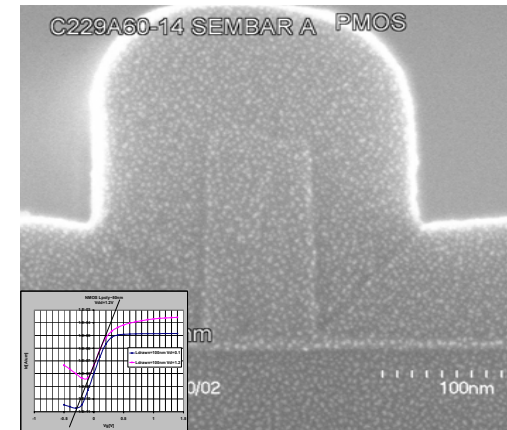
Current Practice



Bulk/PDSOI Aggressive Device Scaling



Fully-Depleted SOI



- Exploratory Device Research

"FinFET scaling to 10nm gate length" (B.Yu et al)

- Adv. Logic Research

"Nickel silicide metal gate FDSOI devices with improved gate oxide leakage" (Z. Krivokapic, et al)

- Adv. Memory Research

"Quantum-well Memory Device (QWMD)with Extremely Good Charge Retention" (Z. Krivokapic, et al)

- New Materials and Process Integration

"Transistors with Dual Work Function Metal Gates by Single Full Silicidation (FUSI) of Polysilicon Gates" (W.P. Maszara, et al)

AMD U.S. Patents Issued



1998			1999			2000			2001		
Company		No. Patents	Company		No. Patents	Company		No. Patents	Company		No. Patents
1	IBM	• 2,682	1	IBM	• 2,789	1	IBM	• 2,922	1	IBM	• 3,453
2	Canon	• 1,934	2	NEC	• 1,853	2	NEC	• 2,034	2	NEC	• 1,966
3	NEC	• 1,632	3	Canon	• 1,800	3	Canon	• 1,897	3	Canon	• 1,877
4	Motorola	• 1,428	4	Samsung	• 1,544	4	Samsung	• 1,442	4	Micron	• 1,643
5	Sony	• 1,321	5	Sony	• 1,429	5	Lucent	• 1,415	5	Samsung	• 1,451
6	Samsung	• 1,306	6	Fujitsu	• 1,231	6	Sony	• 1,394	6	Matsushita	• 1,447
7	Fujitsu	• 1,205	7	Toshiba	• 1,225	7	Micron	• 1,306	7	Sony	• 1,392
8	Toshiba	• 1,194	8	Motorola	• 1,207	8	Toshiba	• 1,264	8	Hitachi	• 1,283
9	Kodak	• 1,125	9	Lucent	• 1,156	9	Motorola	• 1,203	9	Mitsubishi	• 1,210
10	Mitsubishi	• 1,120	10	Mitsubishi	• 1,089	10	Fujitsu	• 1,169	10	Fujitsu	• 1,208
11	Hitachi	• 1,107	11	Matsushita	• 1,065	11	Matsushita	• 1,150	11	Toshiba	• 1,176
12	Matsushita	• 1,058	12	Hitachi	• 1,020	12	<u>AMD</u>	• <u>1,055</u>	12	Lucent	• 1,119
13	Lucent	• 930	13	Kodak	• 993	13	Hitachi	• 1,046	13	GE	• 1,112
14	Philips	• 845	14	Micron	• 934	14	Mitsubishi	• 1,037	14	<u>AMD</u>	• <u>1,090</u>
15	HP	• 866	15	Philips	• 866	15	Siemens AG	• 932	15	HP	• 982
16	Xerox	• 769	16	HP	• 855	16	HP	• 904	16	Philips	• 882
17	GE	• 729	17	<u>AMD</u>	• <u>825</u>	17	Kodak	• 876	17	Siemens	• 817
18	<u>Intel</u>	• <u>705</u>	18	<u>Intel</u>	• <u>735</u>	18	Philips	• 839	18	<u>Intel</u>	• <u>811</u>
19	Siemens AG	• 631	19	Siemens AG	• 731	19	<u>Intel</u>	• <u>797</u>	19	TI	• 806
20	Texas Inst	• 618	20	GE	• 700	20	GE	• 790	20	Motorola	• 785
21	Sharp	• 611	21	Xerox	• 671	21	Texas Inst	• 692	21	Xerox	• 722
22	Micron	• 580	22	Texas Inst	• 604	22	Sharp	• 619	22	Kodak	• 719
	Nikon	• 580	23	Sharp	• 566	23	Xerox	• 577	23	Bosch	• 705
24	<u>AMD</u>	• <u>560</u>	24	Sun Microsystems	• 565	24	Bosch	• 550	24	UMC	• 596
25	MN Mining	• 557	25	Proctor & Gamble	• 551	25	Fuji Photo	• 549	25	Honda	• 587

In Summary....



- 130nm Bulk now in full production for logic; imminent for Flash
- 130nm SOI Hammer in final qualification
- On Track for 90nm Technology Insertion
 - All equipment for initial 90nm logic is in place
 - Excellent early yields on SRAM evaluation vehicle
 - 90nm Hammer vehicle now in process
 - 90nm Flash in early development; Cu interconnect
- 65nm Development plan defined; experimental work in progress
- Research projects aimed at 45nm node and beyond
 - Logic and Flash memory



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